Code No: RT21053 **R13** SET - 1

II B. Tech I Semester Regular/Supplementary Examinations, Dec – 2015.
DIGITAL LOGIC DESIGN
(Com. to CSE, IT)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)
2. Answer **ALL** the question in **Part-A**
3. Answer any **THREE** Questions from **Part-B**

~~~~~~

PART –A

1. a) Convert $(615.25)_8$ to its hexadecimal equivalent (4M)
   b) Prove that $\overline{\overline{A\bar{B}} + \bar{A} + AB} = 0$ (4M)
   c) Give the comparison between serial adder and parallel adder (4M)
   d) Derive the characteristic equation of a SR Flip-Flop. (3M)
   e) A counter has 14 stable states 0000 through 1101. If the input frequency is 50 KHz, what will be its output frequency? (3M)
   f) Explain about PLA. (4M)

PART -B

2. a) Find the difference of $(3250\text{-}72546)_{10}$ by using 10's complement. (8M)
   b) Perform the following: i) 11010 – 1101
   ii) 101011 – 100110 (using 2's complement) (8M)
3. a) Reduce the following boolean expression to 3 literals.
   $\left[\overline{\overline{CD} + A}\right]$ + A+CD+AB (8M)
   b) Express the following function in sum of minterms and product of maxterms
   F(A,B,C,D) = $\bar{B}$D+$\bar{A}$D+BD (8M)
4. a) Design a 2-bit comparator using gates. (8M)
   b) Draw and explain the operation of 3 to 8 decoder. (8M)
5. a) Construct a JK Flip-Flop using a D Flip-Flop, a 2x1 multiplexer and an inverter. (8M)
   b) Convert SR Flip-Flop to JK Flip-Flop. (8M)
6. a) With neat diagram explain the operation of 3-bit universal shift register. (8M)
   b) Draw and explain 4-bit controlled buffer register. (8M)
7. a) A combinational circuit is defined by the functions
   $F_1(A,B,C) = \sum(3,5,6,7)$
   $F_2(A,B,C) = \sum(0,2,4,7)$
   Implement the circuit with a PLA having 3 inputs, four product terms and two outputs. (8M)
   b) Design a BCD to Excess-3 code converter and implement using suitable PLA. (8M)

||''|'''|''|'|'''||
~~~~~~

Code No: RT21053 **R13** SET - 2

II B. Tech I Semester Regular/Supplementary Examinations, Dec – 2015.
DIGITAL LOGIC DESIGN
(Com. to CSE, IT)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)
2. Answer **ALL** the question in **Part-A**
3. Answer any **THREE** Questions from **Part-B**

~~~~~~

PART –A

1. a) Convert $(12.125)_{10}$ into binary. (3M)
   b) Obtain the simplified expression in SOP form for the following using K-map method. (4M)
   F(A,B,C,D) = $\sum(0,1,4,5,16,17,21,25,29)$
   c) What is meant by encoder? (3M)
   d) List the applications of Flip-Flops. (4M)
   e) Determine the number of Flip-Flops needed to construct a register capable of storing decimal numbers upto 32. (4M)
   f) Explain about PAL. (4M)

PART -B

2. a) Add and subtract in binary. (8M)
   i) 1111 and 1010 ii) 110110 and 11101
   iii) 100100 and 10110 iv) 1101001 and 11011
   b) Explain any two binary weighted codes with example (8M)

3. a) Reduce the following four variable function to its minimum sum of products form. Y = $\bar{A}\bar{B}C\bar{D}$ + ABC$\bar{D}$ + A$\bar{B}$C$\bar{D}$ + A$\bar{B}\bar{C}\bar{D}$ + AB$\bar{C}\bar{D}$ + $\bar{A}\bar{B}$CD + $\bar{A}\bar{B}\bar{C}\bar{D}$ (8M)
   b) Simplify the following boolean function using four-variable map. (8M)
   F(w,x,y,z) = $\sum(1,3,7,11,15)$ + d(0,2,5)

4. a) Design and explain about 4-bit priority encoder. (8M)
   b) Implement the following Boolean function using 8:1 MUX. (8M)
   F(P,Q,R,S) = $\sum m(0,1,3,4,8,9,15)$

5. a) What is a flip-flop? Design basic flip-flop circuit with NAND gates. (8M)
   b) Draw and explain the operation of negative edge triggered JK Flip-Flop. (8M)

6. a) Define a ripple counter. Design a BCD ripple counter. (8M)
   b) Explain the working of 4-bit asynchronous counter. (8M)

7. a) Illustrate how a PLA can be used for combinational logic design with reference to the functions: (10M)
   f_1(a,b,c) = $\sum m(0,1,3,4)$
   f_2(a,b,c) = $\sum m(1,2,3,4,5)$
   Realize the same assuming that a 3x4x2 PLA is available.
   b) Compare PROM, PLA and PAL. (6M)

||''|'''|''|'|'''||
~~~~~~

Code No: RT21053 **R13** SET - 3

II B. Tech I Semester Regular/Supplementary Examinations, Dec – 2015.
DIGITAL LOGIC DESIGN
(Com. to CSE, IT)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answer **ALL** the question in **Part-A**
3. Answer any **THREE** Questions from **Part-B**

~~~~~~

PART –A

1. a) Perform $(28)_{10} - (15)_{10}$ using 6 bit 2's complement representation. (4M)
   b) Convert the given expression in standard POS form. (3M)
   f(A,B,C) = (A+B) (B+C) (A+C)
   c) Explain about parallel adder. (4M)
   d) Define a latch and flip-flop. (4M)
   e) How to load data word ABCD = 1101 in the 4-bit bidirectional shift register in shift left mode. (3M)
   f) Explain about PROM. (4M)

PART -B

2. a) Convert the decimal numbers 250.5, 12.0625, 673.23 to binary, base 8 and base 16. [9M]
   b) Explain any two non-weighted codes with example [7M]

3. a) Reduce the following function using K-map technique. (8M)
   f(A,B,C,D) = $\sum m(0,1,4,8,9,10)$
   b) Implement the following boolean function using AND, OR and inverter gates. (8M)
   F = xy+$\bar{x}\bar{y}$+$\bar{y}z$

4. a) Design 4 line to 16 line decoder using 2 line to 4 line decoders. (8M)
   b) Implement full subtractor using demultiplexer. (8M)

5. a) Show that the characteristic equation for the complement output of JK flip-flop is $\bar{Q}$ (t+1) = $\bar{J}$. $\bar{Q}$ (t) + K.Q(t). (8M)
   b) Convert a T Flip-Flop to D Flip-Flop. (8M)

6. a) Design Johnson's counter using a 2 bit shift register. Draw the waveforms. (10M)
   b) List the applications of shift registers. (6M)

7. a) Implement the following Boolean functions using PAL. (8M)
   w(A,B,C,D) = $\sum m(0,2,6,7,8,9,12,13)$
   x(A,B,C,D) = $\sum m(0,2,6,7,8,9,12,13,14)$
   y(A,B,C,D) = $\sum m(2,3,8,9,10,12,13)$
   z(A,B,C,D) = $\sum m(1,3,4,6,9,12,14)$
   b) Using PROM realize the following expressions. (8M)
   F_1(a,b,c) = $\sum m(0,1,3,5,7)$
   F_2(a,b,c) = $\sum m(1,2,5,6)$

||''|'''|''|'|'''||
~~~~~~

Code No: RT21053 **R13** SET - 4

II B. Tech I Semester Regular/Supplementary Examinations, Dec – 2015.
DIGITAL LOGIC DESIGN
(Com. to CSE, IT)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)
2. Answer **ALL** the question in **Part-A**
3. Answer any **THREE** Questions from **Part-B**

~~~~~~

PART –A

1. a) Perform subtraction $(1110)_2$- $(1010)_2$ using 2' complement method. (3M)
   b) Simplify the expression Z=AB + A$\bar{B}$. $\left(\overline{\bar{A}\bar{C}}\right)$ (4M)
   c) Explain about serial adder. (4M)
   d) Compare synchronous and asynchronous sequential circuits. (4M)
   e) Explain about parallel in serial out shift register. (4M)
   f) What is the maximum range of a memory that can be accessed using 10 address lines? (3M)

PART -B

2. a) Subtract the following numbers using 9's complement and 10's complement. (8M)
      i) 5250 – 321
      ii) 753 – 864
      iii) 3570 – 2100
      iv) 20 – 100
   b) Convert the following: (8M)
      i) $(163.789)_{10}$ = ( )$_8$
      ii) $(101101110001.00101)_2$ = ( )$_8$
      iii) $(292)_{16}$ = ( )$_2$

3. a) Simplify and implement the following POS function using NAND gates. (10M)
      f(A,B,C,D) = $\prod M$ (0,1,2,3,12,13,14,15)
   b) Prove that wx + $\bar{y}$ ($\bar{w}$ + $\bar{z}$) = wx + xz + $\bar{x}\bar{z}$ +$\bar{w}\bar{y}$z if $\bar{w}$x + y$\bar{z}$ = 0. (6M)

4. a) Design a code converter that converts BCD into binary. (8M)
   b) Design a combinational circuit for an octal to binary encoder. (8M)

5. a) Design a D type positive edge triggered flip-flop. Explain the operation of the sequential circuit when CP=1. (8M)
   b) Convert JK Flip-Flop to SR Flip-Flop. (8M)

6. a) Draw and explain the operation of 4 bit ring counter. (10M)
   b) What is the difference between ring counter and Johnson's counter? Explain. (6M)

7. a) Design a combinational circuit using PROM that accepts 3 bit binary number and generates its equivalent Excess-3 code. (10M)
   b) What is ROM? List the different types of ROMs. (6M)

||''|'''|''|'|'''||
~~~~~~